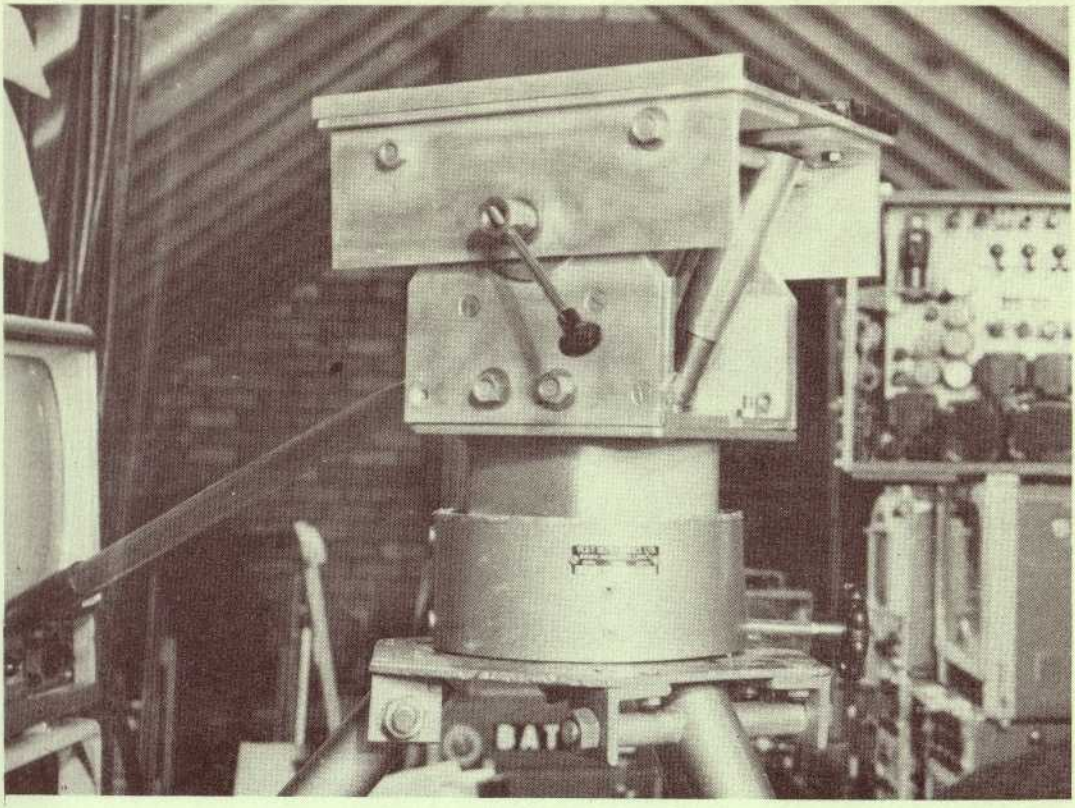

CQ·TV 84

THE BRITISH AMATEUR TELEVISION CLUB.

DECEMBER 1973

THE BRITISH AMATEUR TELEVISION CLUB

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Members wishing to have material published in C Q - T V should send the manuscript and drawings to the Editor; articles are invited on all subjects of interest to amateurs and should be of about 1500 words; larger articles should be divided into convenient Parts for publication in consecutive issues of the journal.

COVER PHOTO An amateur pan tilt head to be described in the next issue.

EDITORIAL

I know it seems very early, but 1974 is almost here and we should be thinking of the B.A.T.C. Convention. The most important decision to be taken is where to hold it, and if any members have ideas on this subject, please let the Hon. Secretary know. Recent venues have been London and Cambridge. How about somewhere new?

Many of you have been looking forward to the reprint of Arthur Critchley's I.C. articles, a booklet which was announced earlier this year. Work is now progressing on this project - all voluntary work, of course - and it is hoped to report a publication date soon. So there is no need to write to us asking "when?" We'll tell you in good time.

It is with regret that we have to record the death of Harold Jones G5ZT. This sad event took place on the 17th August and B.A.T.C. as well as the whole amateur radio world has lost a man who was in the forefront of the hobby. Readers of this journal will know of his slow scan activity; Harold was particularly interested in this mode of transmission, as well as normal fast scan television. On behalf of all members of B.A.T.C. we offer our sincere condolences to his family and friends.

Our President Bob Roberts G6NR has been working very hard since he took office in acquiring redundant stock frm commercial companies for B.A.T.C. members. If you are on the Equipment Registry lists you may well have received some of this yourself. Recently he has come to an arrangement with the BBC over the supply of some unwanted tv equipment, which we hope to be seeing shortly. For our part, the BBC has decided to form a "Museum of Broadcasting" and is looking for suitable exhibits. If you think you have something they could use, or know the whereabouts of anything please let Bob Roberts know, and he could give the BBC some return for their gifts to us! His address is 27 Hill Road, Theydon Bois, Essex.

We have received a letter from Telford Communications of Bridgenorth bringing our attention to their products and services and offering a 5% discount (excluding VAT) to members of B.A.T.C. They offer a range

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of VHF Modules, a 2 metre transmitter, tuneable I.F., 2 metre convertor and accessories and can carry out metal work in 16-18-20swg aluminium, quotation by return on receipt of a sketch and S.A.E. Their address is 78b High Street, Bridgenorth, Shropshire, and mention your B.A.T.C. membership for your discount.

There is a notice on another page reminding you that your subscription is due, and I make no apology for repeating it here! Please don't forget, send your £1 now. With the best will in the world, we can't run B.A.T.C. without your money.

THE EDITOR

POSTBAG

P.Wolfenden VK3ZPA in Victoria, Australia tells of the activity in the Melbourne area which increases week by week, and more with each "demonstration". Four stations are capable of CCIR standards with six more on the way. Distance is a problem and most amateurs tend to concentrate on aerial arrays; even so, noise level is high, about 4 on the B.A.T.C. Reporting Chart system. With 30 miles a common path length this is hardly surprising. Typical equipment in a Melbourne ATV station would be a home brew solid state SPG, a vidicon camera, a transmitter consisting of a grid modulated or series modulated QQE03/20 or QQE06/40 and a Yagi or co-linear. Your suggestion that C Q - T V should have a "Beginners Column" is a good one OM - just as soon as your Editor can find a "volunteer" to write it we'll have one!

E. Garrett G3XHO late of Leighton Buzzard has now emigrated to Australia and when we heard from him was expecting to become VK2BQA quite soon. He also plans to get a /T ticket and with this in mind he has already successfully built an Arthur Critchley SPG and is now building a vidicon camera. Good luck in your new home!

Maitland Lane VK5AO from Henley Beach in South Australia has written with news of activity in his area. Active hams are himself, with VK5ZEF, VK5ZOF and VK50G. In the last year colour pictures have continued to be transmitted, and the groups' record 95 mile contact has been exceeded. Getting married has slowed plans down a little, but a new house soon should mean better things in the future. First duplex working, then maybe a repeater; getting on 1296 is also planned.

G.R. Mather G6AIY/T in Wothing, Sussex is recently licensed /T and hopes to be on the air soon. One other amateur in the area is also licensed, and more are on the way, so perhaps a 70cm net will be operating below the South Downs in the near future - even extending to France!

H.B. Burton G2JR has been operational on SSTV with tapes for some time, but now has a Crofton sampling camera to go with his Robot camera. Tx is a KW Atlanta transceiver and we hope your results are good and get better!

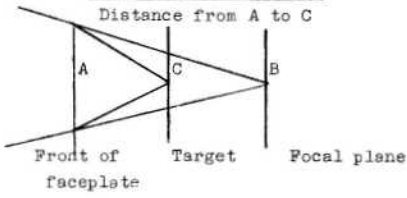
Rick Matthews VK5ZFQ is completing his last year as a student, after which he hopes to get some tv on the air. The C Q - T V SPG is nearly complete, he reports, and soon he will be one of the many in Adelaide currently active on 70cm.

Letters to the Editor

Dear Sir,

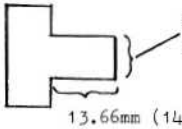
The distance from the front of the lens mount for a "C" mount lens to the focal plane is 17.52mm. To measure that accurately is a bit difficult - but an allowance has to be made for the thickness of the glass face plate and its refractive index. For a typical tube this is 2.362mm, and the refractive index is 1.507. A simple calculation gives Refractive Index =

$$\frac{\text{Distence from A to B}}{\text{Distance from A to C}}$$



This leaves us with the conclusion that the target is slightly in front of the focal plane. For the example quoted:- The faceplate front is 3.55652mm from B (this accuracy is not justified). Hence the distance from front of lens mount to front of faceplate is 17.52 - 3.56 =13.96mm.

I have made a small tool to set this. It is shaped thus:-



13.66mm (14mm is close enough)

We seem to neglect the optics of our hobby, but without the optics the electronics would be of little use!

P.M. Delaney
Reading, Berkshire.

Dear Sir,

Here in the midlands there is a growing interest in slow scan television on 2 metres, so to try to promote this Eddy, G3ZJO of Blisworth, Nr Northampton and myself, (Nr Rugby, in Northants) make a point of being on 2 metres SSB each evening at 7pm around 145.42MHz calling CQ for SSTV and beaming North and South East, if there are any requests to beam in a different direction please let us know. Skeds are also very welcome.

We would like to see an SSTV calling frequency on 2 metres and so we would like to suggest 145.468MHz as this is sufficiently far above the SSB channel for good clearance and also os low enough not to have to change ranges on transceivers. Liner 2s can also cover the frequency.

The RSGB is being approached on this subject but we would like to hear of any objections to this frequency being adopted.

So far we have only contacted a few active SSTVers on two but feel that if more people knew the interest was there then SSTV could well flourish on VHF.

John L. Wood G6AHT/T G3YQC
Rugby, Warwickshire.

A Synchronising Pulse Generator

PETER SHARP G6NNH/T

The operation of an interlaced television synchronising pulse generator is described. It generates waveforms conforming to the CCIR standards. The specification is shown in Table 1.

The unit is intended to be a pulse generator for amateur use, however, the generator is suited to many other television applications.

Series 7400 Integrated Circuits,(IC's), are used throughout with the exception of the descriminator where discrete components are employed. The generator is a dual standard machine capable of 625/525 line operation, the master oscillator operating at a frequency of 31.25KHz and 31.5KHz respectively. Options available but not incorporated in the machine may include external input for "GEN LOCK" and "CRYSTAL" control. Operation for 525/625 line standard is permitted by means of x and y links on the PCB. These control the line divide counts and the divide-by-eleven/thirteen counter.

CIRCUIT DESCRIPTION (625 lines)

For simplicity pulse timings are achieved by means of monostables. Suitable combinations of the timing components give the required timings for Field Drive, Field Blanking, Syncs etc. thus avoiding the need for complex dividers. However, it is necessary to use one divider chain. Table 2 gives the monostable components which may be modified to obtain any standard required. A block diagram is shown in Fig. 8.

SERRATION PULSES

The output of the master oscillator, twice line frequency, is fed to the first monostable producing pulses of 4.7 microsecond duration. These pulses are used to generate the field sync serrations pulses. Referring to Fig. 15 the waveform is as shown at (B) and all other pulses are initiated by these pulses. The waveform shown as O/P Fig. 15, shows that the rising-edges of the half-line equalising pulses and sync pulses must coincide with the rising edges of the broad pulses to maintain correct synchronisation of the line oscillator during

the field sync period. Therefore, it is necessary to generate the serration pulses prior to the start of the line sync pulses. These serration pulses are gated at a later stage in the circuit so that they appear only during the field sync period.

LINE COUNTER

Four counters, (IC's 1,5,9 and 13), are used to divide the twice-line frequency by 625 to obtain the Field Drive and Blanking frequencies.

The output of the line counter is a 4.0 millisecond pulse and drives two monostables which produce a Field Blanking pulse of 1.6 milliseconds (25 lines), and a Field Drive pulse of 480 microseconds. The 480 microsecond pulse corresponds to 7.5 lines. This is also used as a control gating waveform to initiate the field sync generation. .. third output of this pulse is applied to the master oscillator discriminator for comparison with the mains frequency of 50Hz so that mains locking may be achieved.

BLANKING

The Q-output of the serrations monostable is coupled to a divide-by-two counter and a delay monostable whose pulse width is 3.2 microseconds. The divide-by-two counter consists of a dual D-type edge-triggered bistable type SN7474 and produces the waveform at (C) Fig. 14. The pulse from the delay monostable at (E) Fig. 14 is combined in a NAND-gate with the output of the divide-by-two counter to produce 3.2 microsecond pulse at line frequency which is then used to trigger a monostable which generates the 12 microsecond line blanking pulse shown at (F) Fig. 14. Mixed Blanking is obtained by adding Line and Field Blanking pulses in another NAND-gate.

The generation of the front porch of 1.5 microseconds is achieved by an unusual method whereby the line synchronising pulse is delayed by 1.5 microseconds with respect to the leading edge of the Line Blanking pulse. Since the Line Sync pulses occur 4.7 microseconds after the start of the serration pulses, a delay of 3.2 microseconds from the same leading edge will give the correct timing for the Line Blanking pulse. See Fig.14 (B). Line Sync is generated from the trailing edge of the serration pulses. During the Field Sync period, the sync pulses appearing at (H) Fig. 14 are inhibited by the field Drive to the input of the Line Sync generator, IC 15. See also (H) Fig. 15.

Fig. 1 shows an oscillogram of the Mixed Blanking waveform relative to the Mixed Sync output. The picture is a little small and it is rather difficult to see that the Blanking is half a line out of sync. This is due to an error which was un-noticed at the time by having the 'scope' on 'alternate' rather than 'chopped'. However, a complete line period is shown in Fig. 2 where the line sync has been algebraically added to the blanking on the 'scope'.

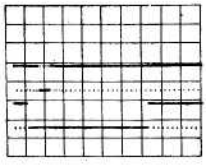


Fig.1. Upper Mxd Sync
Lower Mxd Blkg
2v/cm.

SYNCS

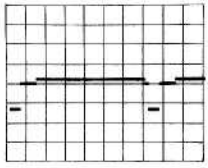


Fig.2. Comp Sync/Blkg 2v/cm.

The $\bar{Q}$-output of the divide-by-two counter drives a 4.7 microsecond monostable whose output is the Line Sync at (H) Fig. 14. A further putput from IC20 NAND-gate gives a Line Drive of 6.6 microseconds advanced by 1.5 microseconds on the Line Sync. The $\bar{Q}$-output of the serrations generator drives a monostable generating the equalising pulses of 2.3 microseconds duration. These pulses are gated out as part of the Field Sync. Fifteen equalising pulses only are generated and appear at the output of IC 8, (I) Fig. 15. Gating of the equalising pulses is achieved by applying inverted Field Drive to A1, A2 inputs of the monostable IC 8. Since the output syncs have to occur at line frequency, then the gating waveform which appears at the output of the divide-by-two line counter has to be applied to the A1, A2 inputs of the line sync monostable to ensure that the monostable is only triggered once every two half-lines.

FIELD SYNC

Refer to Figs. 9 and 15. One half of a dual D-type edge-triggered bistable type SN7474 is used as a latch. Its purpose is to allow 11 or 13 serration pulses of 4.7 microsecond duration through a NAND-gate to the divide-by-eleven/thirteen counter. The operation of this counter will not be described for the moment but the resulting waveform is shown at (P) Fig. 15. A brief analysis of theoperation of the latch is shown in Fig. 13. The purpose of the counter is to obtain a gate which will allow five equalising pulses through a gate in the low state and five serrations through a gate in its high state. The combination of equalising and serration pulses is then fed through a system of gates, IC 16. At a count of eleven, the latch bistable is reset inhibiting the gate and thus removing clock pulses to the divide-by-eleven counter input.

The first five equalising pulses are determined by the counter in the low state and the serrations by the counter in the high state and the last five equalising pulses by the finish of the Field Drive period. The waveforms obtained are as at (H), (I), ($\bar{P}$) and (K) and by a combination of these the result is at (O/P).

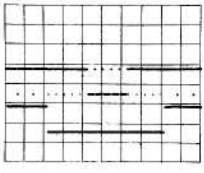


Fig.3.
Field Sync. Even Fields
2v/cm.

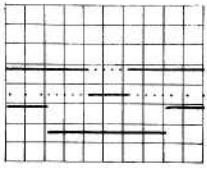


Fig.4.
Field Sync. Odd Fields
2v/cm.

525 Line Standard Circuit Description

The operation for 525 lines is basically the same as for 625 but with the exception of two main differences. The line divider has now to divide by 525 from the master oscillator frequency and the divide sequence is therefore 7,3,5,5. The first two line divide counters IC 1 and IC 5 can be made to divide by 7 or 5 and 3 or 5, see Fig. 10. Inserting link x gives 625 and y 525 line standard.

The Field Sync is also different although the waveform to that shown at (O/P) Fig. 15 is basically the same. For 525 line operation the first and second series of equalising pulses plus the broad pulses should now be each 3 line long.

This means that two extra equalising pulses and one serration pulse is required. This is achieved by earthing off the RO reset gate to IC 12 through IC 16 so that the divide-by-eleven counter now counts by twelve. A 1 pulse delay is inserted into the count sequence to enable six equalising pulses to be inserted into the Field Sync period instead of five.

POWER UNIT

The simple power unit comprises a transformer capable of delivering the total current requirement of 330mA and a voltage reulator type MLM309K. Use of a 1000 microfarad smoothing capacitor gives 1.5 volts of ripple to the input of the regulator. The output regulation is less than 5 millivolts of ripple.

CONCLUSION

No mention has been made of the master oscillator although in Fig. 11 the use of an SN7413 is made. This was a very recent addition to the generator as all previous prototype generators have used discrete components up until now very successfully. Line drivers also are as recent addition since conventional emitter followers using discrete components were used in the past. A suitable "GEN LOCK" circuit is under development and will be included in C Q - T V at some future date.

Facilities are included in the generator for modification to colour. The additions are the use of the second half of the SN7474 bistable for production of Line Ident etc. This will also appear in a future edition of C Q - T V.

All parts for the generator can be supplied as individual items or in kit form or ready made by contacting the Editor B.A.T.C. A circuit diagram of the original M.O. is in Appendix A.

ACKNOWLEDGEMENTS

The author wished to thank the Directors of Plessey Radar Limited, for permission to publish this article.

The author would also like to extend his gratitude to Mr. A.W. Critchley of EMI Electronics Limited for his comments and views on this article.

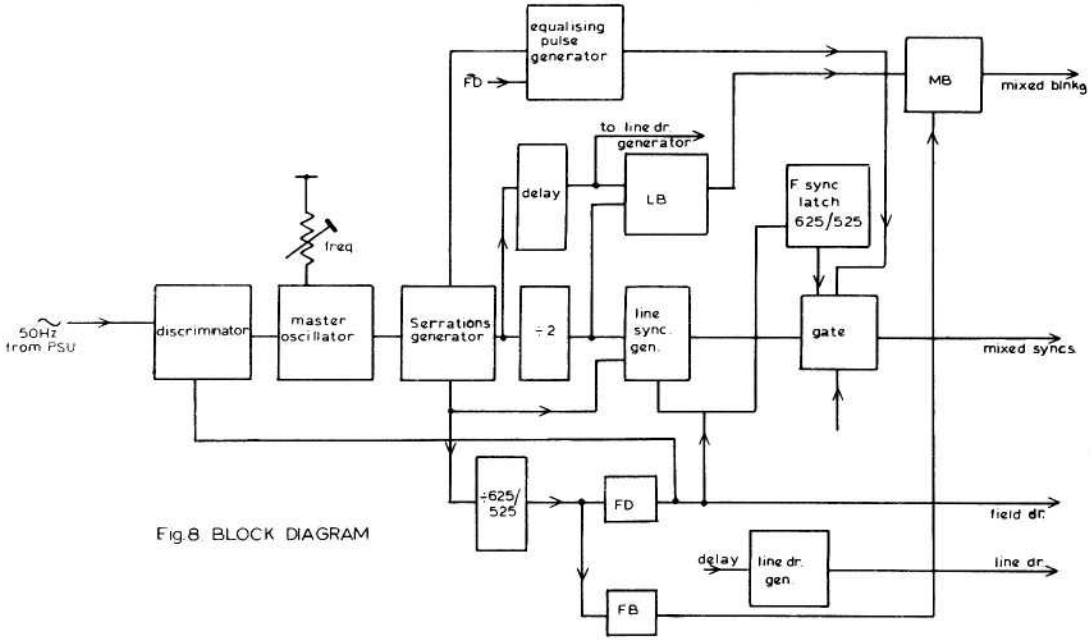
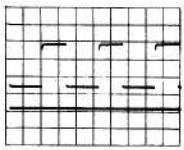


Fig.8 BLOCK DIAGRAM

APPENDIX A

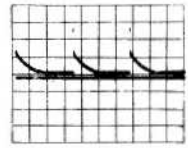
The Master Oscillator is an emmitter coupled voltage controlled oscillator coprising TR1 and TR2. The resultant square wave output from TR3 is directly connected to the serrations generator at twice line frequency. For good temperature stability a polycarbonate capacitor of 6.8nF is used. Frequency is governed by RV1 and is adjusted in conjunction with the mains reference via the discriminator.

The mains supply reference input of 8 volts is compared with the output of the 625 line divider output at the junction of D1 and D3. D3 removes the negative half of the reference so that the oscillator locks onto the positive half of the reference only. Filtering is achieved by C2, C6 and C3 to obtain a small positive or negative swing at the base of TR1.



Master Osc. Output (TR3)
10 µS/cm 2v/cm Fig.5.

Master Osc. TR2 Emmitter
10 μS/cm 2v/cm Fig.6



Master Osc. TR1 Emmitter
10 μS/cm 2v/cm Fig.7.

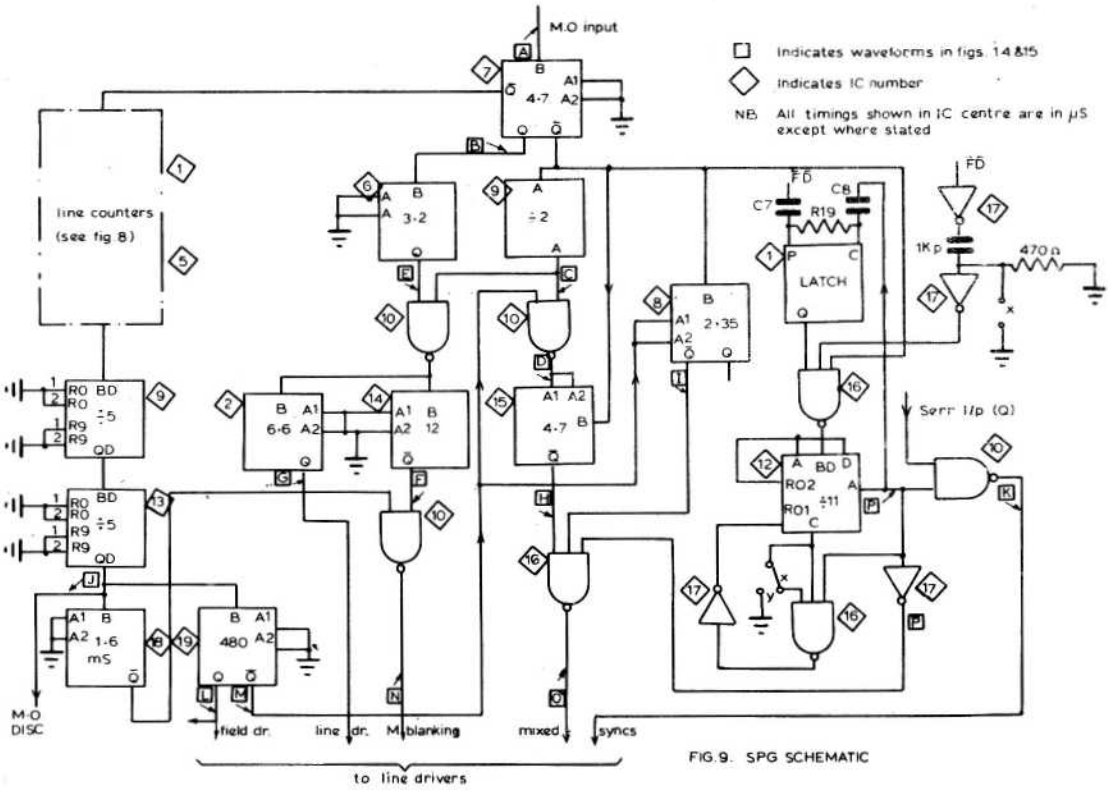


FIG.9. SPG SCHEMATIC

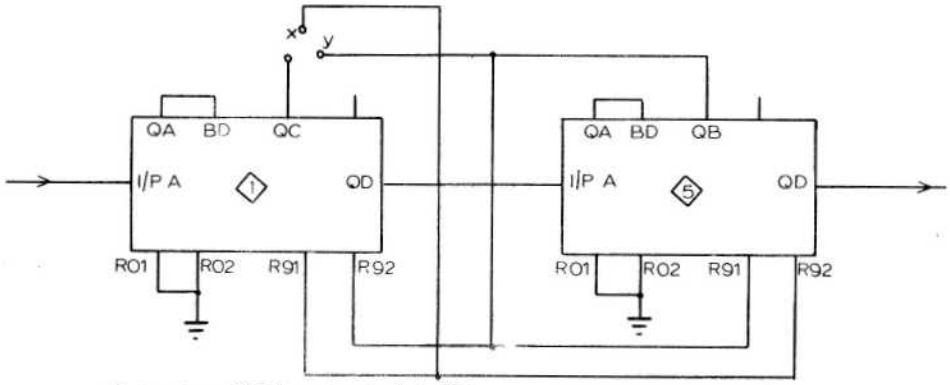


FIG.10. MODIFICATION OF FIRST TWO LINE DIVIDE COUNTERS FOR 525/625 STANDARD

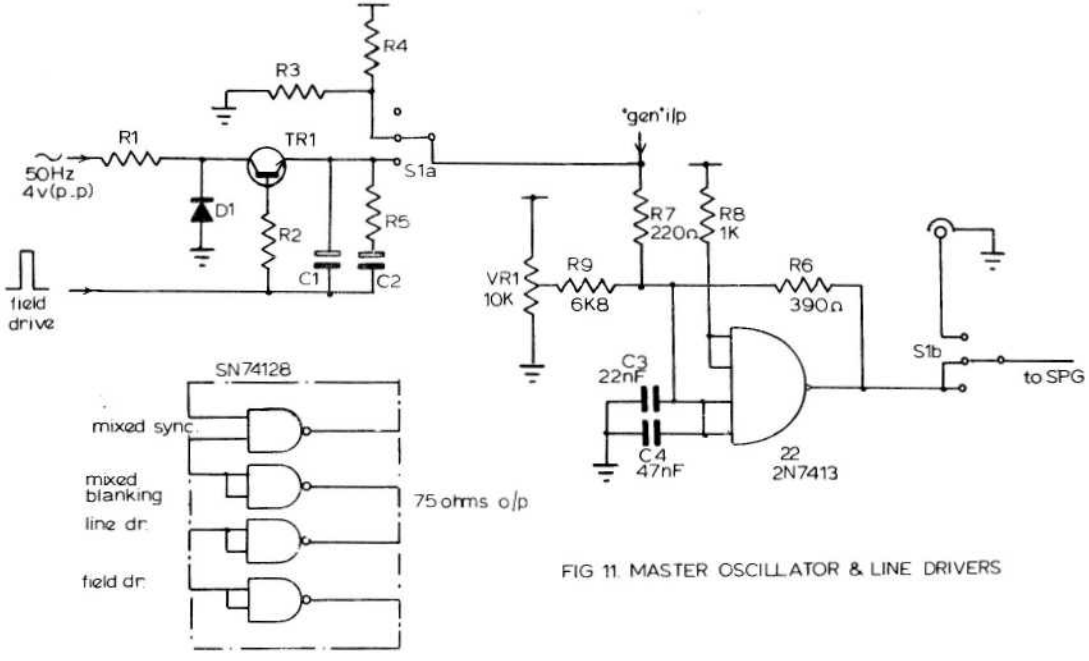


FIG 11. MASTER OSCILLATOR & LINE DRIVERS

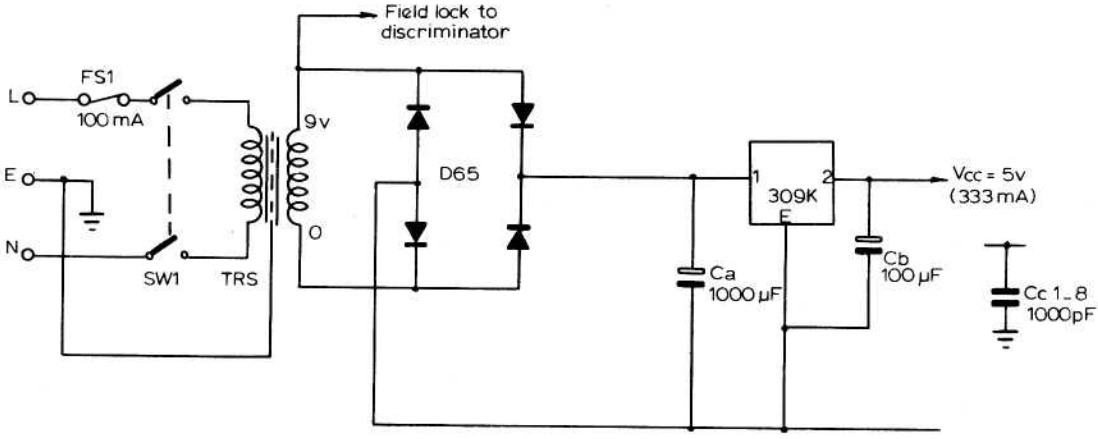


FIG. 12. POWER SUPPLY

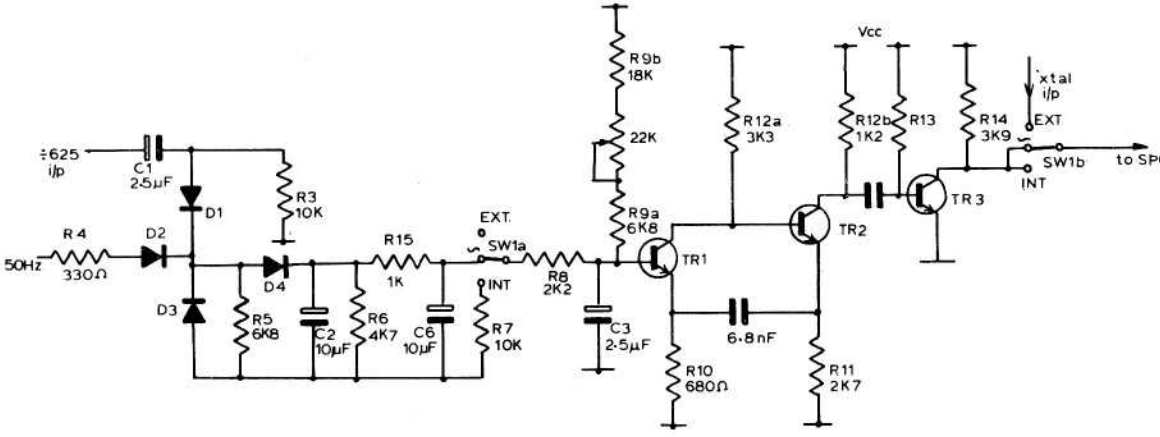


FIG. 16. MASTER OSCILLATOR (ALTERNATIVE)

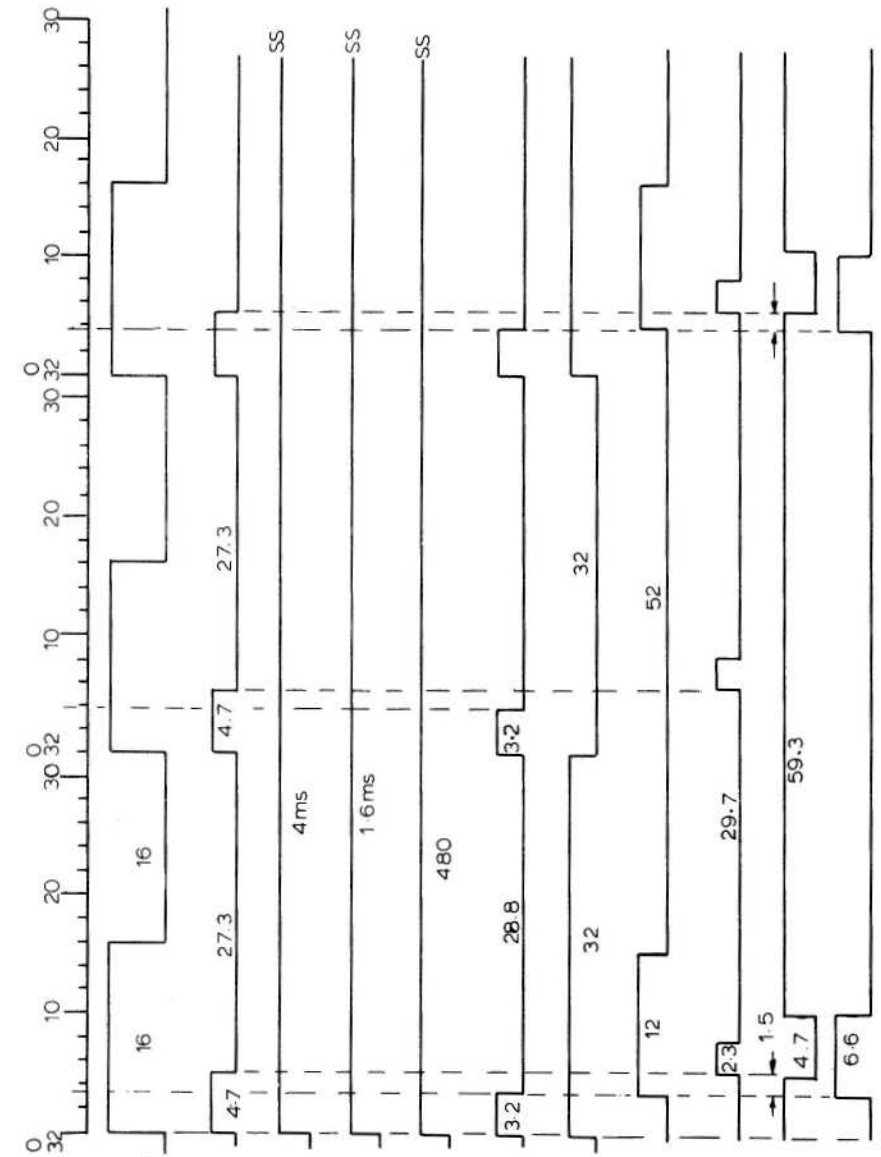


FIG. 14 MAIN TIMING

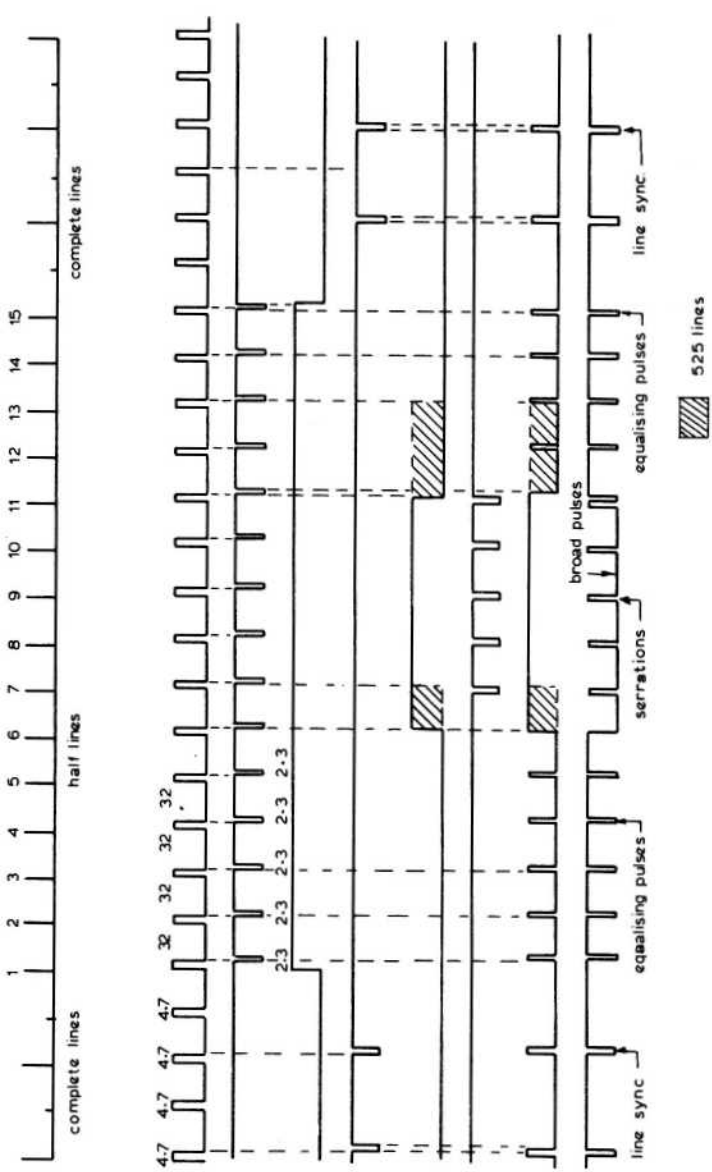
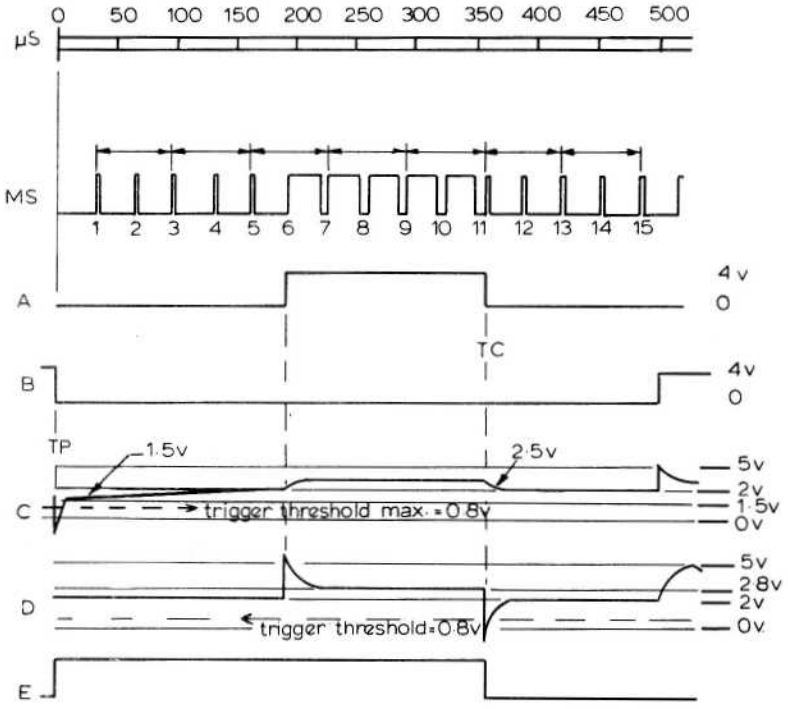


FIG.15. GENERATION OF FIELD SYNC PULSE.



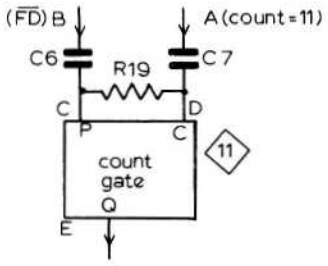


FIG.13. OPERATION OF COUNT GATE

TABLE 1

SIGNAL	SYSTEM M (525)		SYSTEM D K K1 (625)	
LINE PERIOD	63.5uS	RISE TIMES	64uS	RISE TIMES
LINE BLANKING	(10.2-11.4) - 10.8	300nS ± 100nS	(11.8-12.3) -12.05	300nS ± 100nS
LINE SYNC. PULSE	(4.19 - 5.7) - 4.95	250nS ± 100nS	(4.5-4.9) -4.75	225nS ± 75nS
FRONT PORCH	(1.27-2.54) - 1.9		(1.3-1.8) -1.55	
FIELD BLANKING	(19-21 HO - 20H	300nS ± 100nS	(2.5H)(1.6mS)-25H	300nS ± 100nS
1ST EQUAL SERIES	3H		2.5 or 3H	
2ND EQUAL SERIES	3H		2.5 or 3H	
F. SYNC.	3H		2.5 or 3H	
EQUAL PULSES	(2.29-2.54) - 2.42		(2.25-2.45)-2.35	
F. SYNC. DURATION	(26.4-28) - 27.2	300nS ± 100nS	(2.5H) -160.0	300nS ± 100nS
F. SERRATIONS WIDTH	(3.8-5.6 -4.7	300nS ± 100nS	(4.5-4.9) -4.7	300nS ± 100nS
LINE DRIVE	-5.8	300nS ± 100nS	-6.6	300nS ± 100nS
FIELD DRIVE	(9H) -571.5	300nS ± 100nS	(7.5H) -480.0	300nS ± 100nS
OUTPUTS MB	4v p-p negative	into 75		
MS	4v p-p negative	into 75		
LD	4v p-p negative	into 75		
FD	4v p-p negative	into 75		

NOTE: All Times in uS except where stated.

TABLE 2

	C		R		t		
IC. NUMBER FUNCTION	525	625	525	625	525	625	TYPE
2 LINE DRIVE	P560pf	P680pf	18.oK	18.oK	5.8uS	6.6uS	74121
6 DELAY	P470pf	P470pf	10.0K	10.0K	3.5uS	3.5uS	74121
7 FIELD SYNC.	P1000pf	P1000pf	6K8	6K8	4.7uS	4.7uS	74121
8 EQUAL'G.PLS'S.	P470pf	P390pf	8K2	8K2	2.4uS	2.3uS	74121
14 LINE BLANKING	P1000pf	P1000pf	15K	18K	10.8uS	12.0uS	74121
15 LINE SYNC.	P1000pf	P1000pf	8K2	6K8	4.95uS	4.7uS	74121
18 FIELD BLANKING	HO.1mF	HO.1mF	22K	27K	1.28mS	1.6mS	74121
19 FIELD DRIVE	HO.1mF	HO.1mF	12K	8K2	571.5uS	480uS	74121

P = POLYSTYRENE DC = DISC CERAMIC H = MULLARD HUMBUG R = 5% Tol.

CIRCUIT NOTEBOOK No15

J. Lawrence GW6JGA'T

CAMERA TUBES & POWER SUPPLIES

Vidicon Tubes

The most popular type of Camera Tube in use by Amateurs today is the magnetically scanned Vidicon.
The operation of the Vidicon is well described in Manufacturers publications (1) (2) (3).
It is available with either an integral mesh or separate mesh connection. The separate mesh tube is capable of superior performance, particularly in definition, and is the type currently available from the B.A.T.C.
However, there are still many integral mesh tubes about and information on both types is given in Fig. 1.
It is possible to fit an integral mesh tube in a camera designed for separate mesh operation but in the reverse situation it is very important not to connect the Mesh, G4, to the wall anode, G3, but to a potential preferably at least 20 volts higher than the limiter G2.
Mullard Ltd. publish a leaflet giving details of the modifications required (4).

Plumbicon Tubes

Plumbicon Tubes which are very similar in operation to Vidicon tubes are just beginning to appear on the Amateur Television market and information is included on this type of tube.
The Plumbicon has several advantages over the Vidicon and is capable of producing high definition pictures virtually free from shading and lag.
Plumbicon tubes are usually larger in diameter (30.15mm) than the Vidicon and a matching scanning yoke is needed, also somewhat more scanning power is required.
In the Vidicon tube the target voltage may be increased to provide an increase of sensitivity and this voltage can be used as a means of manually or automatically controlling the sensitivity of the camera to suit changes in lighting conditions.
The Plumbicon tube however, due to the different type of target material, does not exhibit this effect and the target voltage is normally set to a predetermined voltage and sensitivity is controlled by the lens iris or a neutral density filter or wedge.
The D.C. supplies to the Vidicon or Plumbicon tube should incorporate adequate decoupling as stray pick-up from the mains supply and scanning circuits may cause shading and other

Electrode	Target	Mesh	Wall anode/ Beam Focus	Limiter/ Accellerator	Cathode	Modulator/ Grid
Mullard Symbol	Target	A3	A2	A1	K	G
EMI & EE Symbol	Signal Electrode	G4	G3	G2	K	G1
Integral Mesh Vidicon e.g. EMI 10667	+15v to -100v	Internally Connected to G3	+250v to +300v	+300v	0v +10v Blank'g	0v to -125v
Separate Mesh Vidicon e.g. EMI 9677/9728 E.E. P849	+10v to +60v	+320v to +450	+280v to +300v	+300v	0v +10v Blank'g	0v to -100v
Separate Mesh Vidicon, as above. High Voltage Operation	+10v to +60v	+750v	+400v to +500v	+300v	0v +20 Blank'g	0v to -100v
Plumbicon e.g. Mullard 55875	+25v to +45v	Internally Connected to A2	+550v to +650v	+300v	0v +25 Blank'g	0v to -100v

The above information is a guide only and has been extracted from the Manufacturers Data Sheets which should be read in detail for full information and setting-up procedure.

Fig. 1.

defects in the picture.

For simple cameras (5) the tube supply voltages can be obtained from a mains transformer with rectification and suitable filtering as shown in Fig. 2, but should the mains supply voltage vary it may be necessary to readjust the tube controls.

For more sophisticated cameras, it is usual to stabilise the supplies to the tube and this will provide drift free operation over long periods. An example of a stabilised D.C. to D.C. convertor supply operating from a 12 volt regulated supply is shown in Fig. 3 (6).

This supply is capable of operating a separate mesh Vidicon tube in the "High Voltage" mode giving a further increase in resolution.

In any case it is very desirable to stabilise the focus coil current by using some form of constant current supply.

A simple circuit, as shown in Fig. 4 is often adequate but for greater stability a more elaborate constant cureent supply should be used, as shown in Fig. 5 (8) (9).

R Plumbicon is a registered trademark.

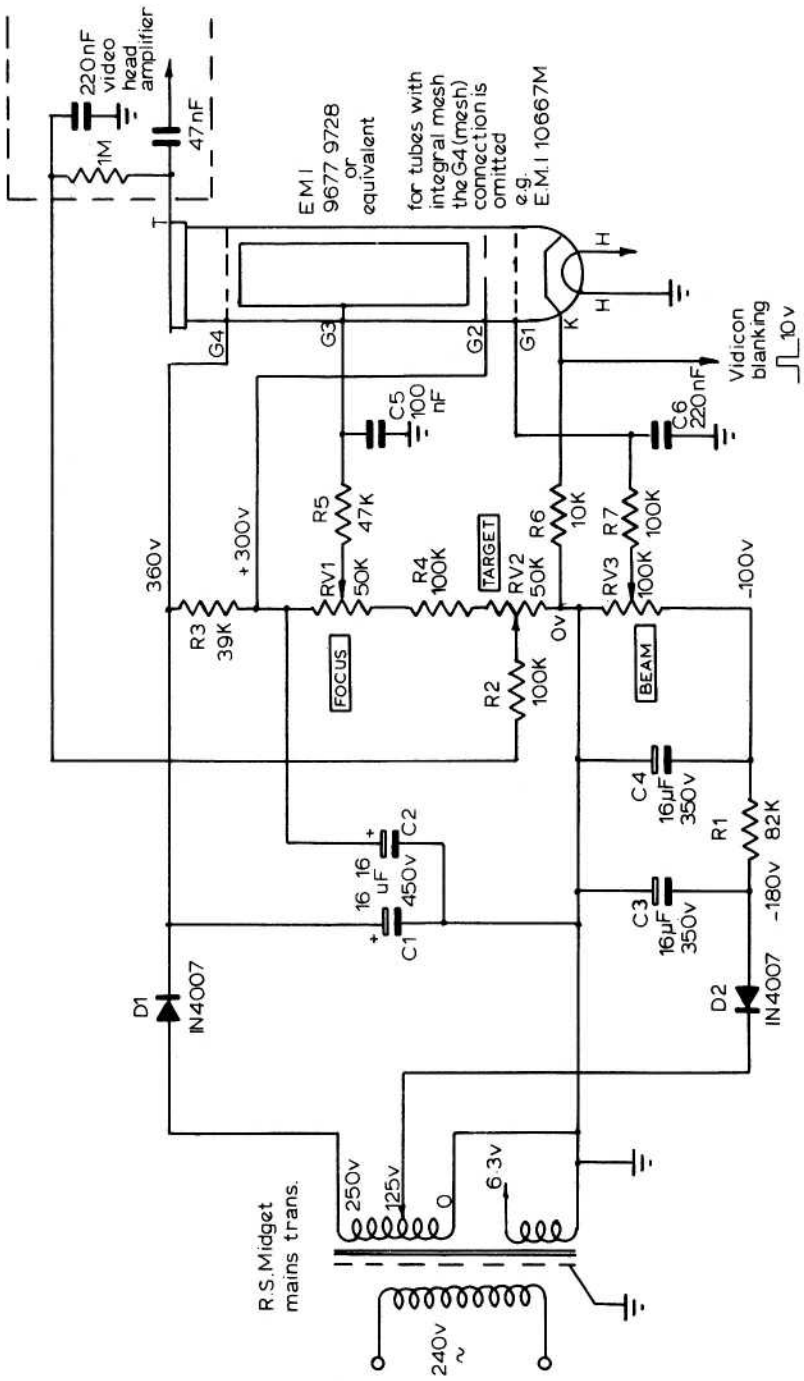


Fig.2. Vidicon tube supplies for a simple camera

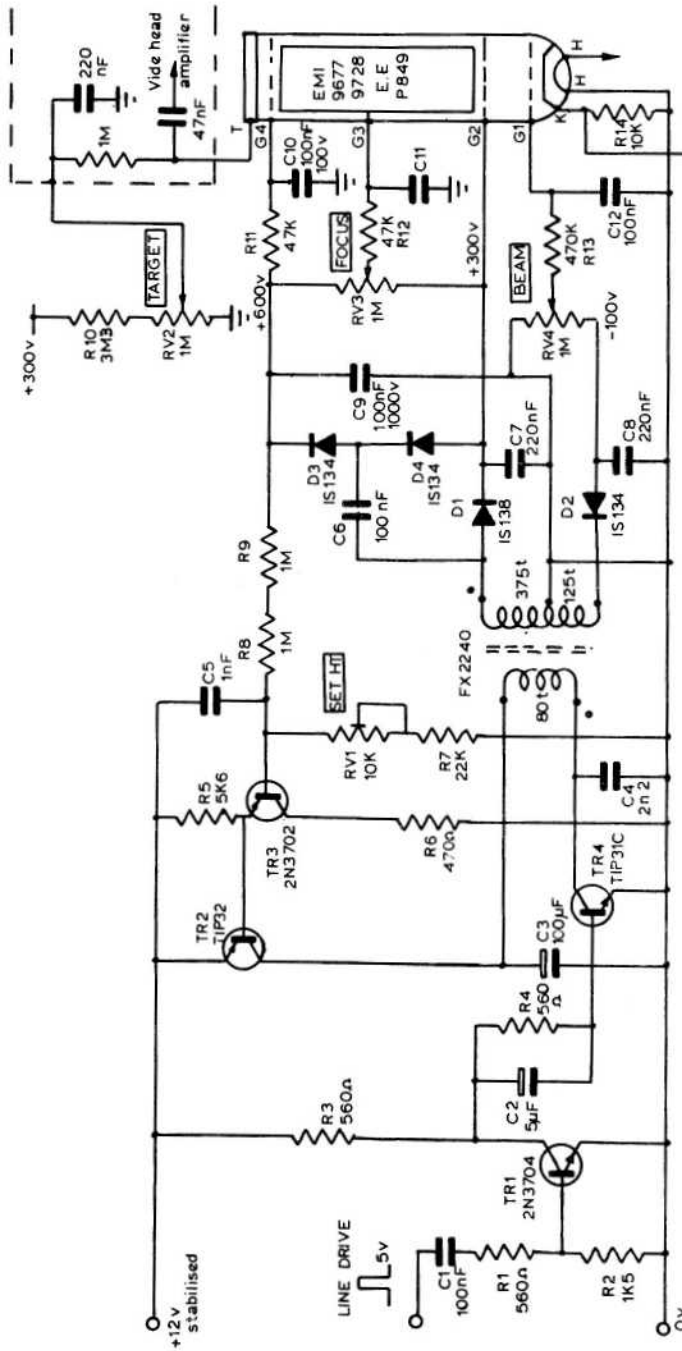


Fig.3. D.C._D.C convertor, stabilised H.T supply, for vidicon operating in high voltage mode

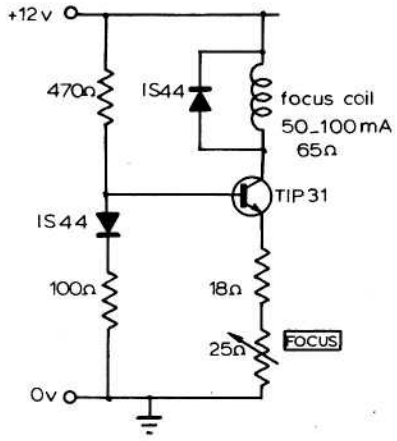


Fig. 4. Simple focus current regulator

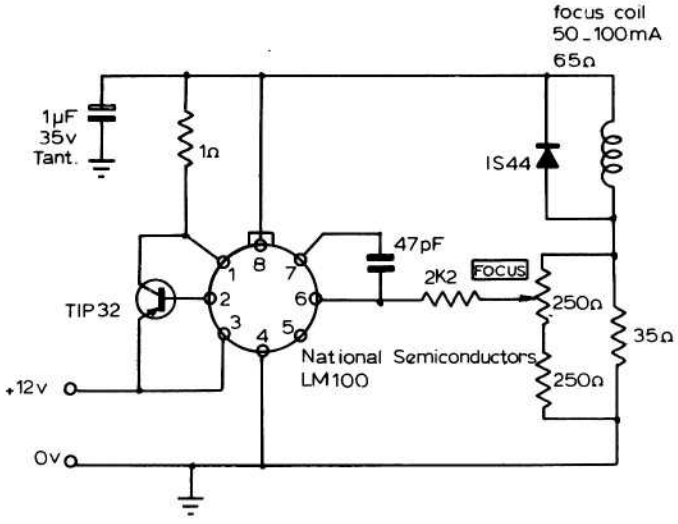


Fig. 5. Precision focus current regulator

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Note:- Data Sheet for the 9677/9728 Vidicon is available from E.M.I. Electronics Ltd.
Data sheet for the P849 Vidicon is avialable from the English Electric Valve Co. Ltd. Chelmsford, Essex.

INTEGRATED CIRCUITS PART 14

A.CRITCHLEY Dip El; C Eng; MIERE.

LOGIC, BOOLEAN ALGEBRA, KARNAUGH MAPS & COUNTER DESIGN

Introduction

Now that digital Integrated Circuits are commonplace it is frequently the case that logic circuit descriptions include such expressions as AND, OR, 0,1, $A\overline{B}$, and so on. This article, the last in the series about TTL IC's, attempts to clear up some of the mystery and also shows how to design counters with the aid of Karnaugh Maps.

The Binary system.

An essential part of the understanding of digital circuits is a knowledge of the Binary System of numbers. There are many numbering systems such as the usual decimal, octal(8), or even alphabetical (26) but the binary system is the simplest in that it uses the fewest numbers - just two. It is based on the most simple principle too - a thing either is or is not. The objects concerned are of no real importance, but in electronics voltage and no voltage are usual, represented by 1 and 0 respectively. Thus 1 represents ON and 0 represents OFF.

Counting in the decimal system involves going through the sequence of numbers until they are used up and then placing the first number (1) down whilst the entire set is again gone through. This first number is then changed for the second number and so on, as far as necessary.

i.e. 0,1,2,3,....8,9,10,11,12,13,....18,19,20,21,...etc.

This principle applies equally well to all other numbering systems, including the binary one.

i.e. 0,1,10,11,100,101,110,111,1000,1001,1010,1011,.....

The numbers soon get used up and the length quickly grows.

Inspection of this sequence reveals that all numbers with a 1 followed by all 0s are powers of 2 (decimal). In fact the number of 0s gives the power. This is a useful fact when converting from binary to decimal and vice versa as the various 1s representing these powers can be summed together. This is shown in the diagram following.

Binary	Decimal	
0	0	
1	1	2^0
10	2	2^1
11	3	
100	4	2^2
101	5	
110	6	
111	7	
1000	8	2^3
etc		

Conversely, these powers of two are successively subtracted starting with the highest until the remainder is zero.

Thus:-

Binary $1011010 = 1.2^6 + 0.2^5 + 1.2^4 + 1.2^3 + 0.2^2 + 1.2^1 + 0.2^0$

$= 2^6 + 2^4 + 2^3 + 2^1$

$= 64 + 16 + 8 + 2$

$= 90$ in decimal.

Decimal $45 = 32 + 13$ or $2^5 + 13 = 100000 + 13$

$13 = 8 + 5$ or $2^3 + 5 = 1000 + 5$

$5 = 4 + 1$ or $2^2 + 1 = 100 + 1$

$1 = 1 + 0$ or $2^0 + 0 = 1$ remainder zero

The binary total is 101101

Binary numbers can be added, subtracted, multiplied and divided just like decimal numbers but for logic use we are limited to addition and multiplication with occasional subtraction - which can be performed by adding anyway.

Addition can be thought of as OR and multiplication as AND as we shall see in a moment.

Venn Diagrams (Sets and Groups)

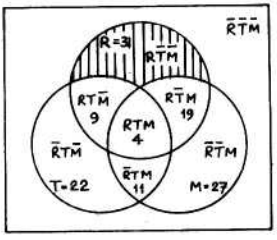
A common kind of problem goes something like this :-

A company has three divisions, Radio, Television & Motors and a staff of 48 salesmen. In a year 31 of them sold their quota of radios, 22 their TVs, 27 their motors, 9 both radios and TVs, 11 both TVs and motors and 19 sold radios and motors whilst 4 sold all three. How many sold only radios and how many should be sacked?

Rather a puzzler but not too difficult with the aid of logic and a particular method of displaying logic known as a VENN diagram. This sort of problem and solution is literally childs play as primary schoolchildren are taught about such things nowadays. The problem is similar in a way to those found in digital circuitry and requires the manipulation of AND and OR functions.

A Venn diagram can be drawn to represent the various conditions. The rectangle represents the set of 48 salesmen and one circle the number who, altogether, sold radios. A second circle represents those selling TVs and a third those selling motors. The circles overlap because some salesmen sold more than one kind of device. The area outside a circle therefore represents salesmen selling anything else other than the device that the circle refers to. The area around the whole of the circles must then be salesmen who sold nothing. The intersecting area of two circles is the portion of those two types of salesmen who sold both devices and so on. Each of these areas is known as a subset.

Since R represents radios, no radios can conveniently be shown by $\bar{R}$ (NOT-R) and similarly for the others.



The overlapping portions of these circles tell us how many units are sold by the various salesmen.

Thus R & T only is $R\bar{T}\bar{M} - RTM = 9 - 4 = 5$

Similarly, Radios & motors only = $R\bar{T}M - RTM = 19 - 4 = 15$

TVs and motors only = $\bar{R}TM - RTM = 11 - 4 = 7$

So to find those selling radios only we take :-

Subset R - (subsets $R\bar{T}\bar{M}$ & RTM & $R\bar{T}M$) (the shaded area)

$= 31 - ((9 - 4) + 4 + (19 - 4))$

$= 31 - (5 + 4 + 15) \quad = 31 - 24$

so $R\bar{T}\bar{M} = 7$

How many should be sacked? Well, it can be shown that $R\bar{T}\bar{M}$ & RTM are 6 and 1 respectively so that the total area enclosed by the circles is :-

$R\bar{T}\bar{M} + \bar{R}T\bar{M} + \bar{R}\bar{T}M + R\bar{T}M + \bar{R}TM + R\bar{T}M + RTM$

$= 7 + 6 + 1 + 5 + 15 + 7 + 4 \quad = 45$

and so 3 salesmen should be sacked.

The Venn diagram is seen to be a pictorial representation of logic and certain expressions are used which are also used in electronic logic .

Some conclusions can be drawn from the logic. For example, a Group is said to exist if elements exist in any one of the subsets of that group.

i.e. G = 1 if S1 OR S2 OR S3 = 1, or G = S1 + S2 + S3

(the plus sign does not mean addition but OR)
Also, a subset such as $R.\bar{R}$ cannot contain elements since a salesman cannot both sell and not sell radios.

i.e. $G = R.\bar{R} = 0$

A subset $R + \bar{R}$ must contain elements as every salesman either does or does not sell radios and the group containing both must exist.

so $G = R + \bar{R} = 1$

Similar reasoning leads to all kinds of equations and formulæ. Some are:-

$R.R = R$, $R + 1 = 1$, $RT + RL = R(T + L)$, $R + RM = R$ etc, etc.

These conclusions form the basis of Boolean Algebra (invented by George Boole 1815 - 64) and can be proved by working out various areas on the Venn diagram.

Boolean Algebra

This seems to be very strange at first sight as it has only three operators called AND, OR and NOT. These are written as:-

A AND B is A.B, or AB, and means A multiplied by B.
A OR B is A + B and means the sum of A and B
NOT A is $\overline{A}$ meaning inversion.

Boolean Algebra is an extension of Sets and Groups and Venn Diagrams and enables digital logic to be expressed in a simple manner on paper.

For instance, if either one of two quantities must be present for a system to work then this is A OR B = Y. In Boolean Algebra this is written as A + B = Y. If both must be present then A AND B = Y and this is written as A.B = Y. If A must be absent then NOT A = Y and this is written as $\overline{A}$. Similarly, if $\underline{A}$ has to be present whilst B is absent this becomes $A.\overline{B} = Y$.

There are laws to be followed concerning the two states 0 and 1. Y is either 0 or 1 as are A and B and any other variables, but this is not the place to go into great detail about it all. Any book on Boolean Algebra will give a list of useful relationships.

Some of the most useful identities are given below.

$A + A = A$, $A + 1 = 1$, $A + 0 = A$, $A.0 = 0$, $A.1 = 1$,
$A.A = A$, $A.\overline{A} = 0$, $\overline{\overline{A}} = A$, $A + \overline{A} = 1$, $A + AB = A$,

There is a very useful one known as De Morgan's theorem which states that :-

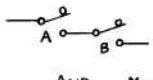
$$\overline{A.B} = \overline{A} + \overline{B} \qquad \text{or} \qquad \overline{A + B} = \overline{A}.\overline{B}$$

This is seen to be a way to change an AND type of expression into an OR type; and vice-versa. It is extremely useful when trying to minimise the amount of logic required in a system; as will be seen shortly.

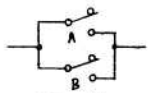
Any number of variables can be combined of course, not the one or two shown so far.

Switching Logic

Boolean Algebra is ideally suited to the logic of switching circuits such as relays. AND and OR are easily interpreted as :-



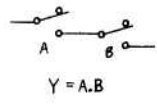
AND $Y = A.B$



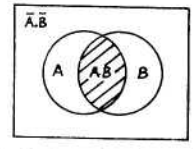
OR $Y = A + B$

NOT is also possible:-

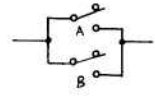
Each circle in a Venn diagram can be thought of as being a switch contact condition and the surrounding area as its NOT condition. A subset A.B therefore represents the condition that $\underline{\text{both}}$ A and B are ON together.



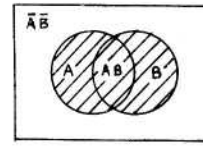
$Y = A.B$



This is expressed in Boolean Algebra as $Y = A.B$ as we have already seen. Similarly $Y = A + B$ is seen to be:-



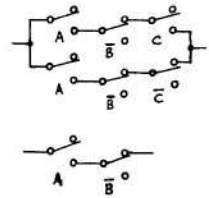
$Y = A + B$



Note that this includes the portion A.B

The Venn diagram is useful but as soon as the number of variables gets over two it becomes a mess with some very awkward shapes and a better way to display the information is desirable. One method, called a Karnaugh Map, will be investigated shortly. For the moment, though, it evident that Boolean Algebra can be used to write down on paper a description of a switching logic system. Furthermore, by applying the rules of Boolean Algebra the system can very often be simplified - or minimised to use the usual term. This can be done $\underline{\text{before}}$ the circuitry is even drawn.

For example, a switching system looks like this :-



The Boolean expression for this arrangement is $A.\overline{B}.C + A.\overline{B}.\overline{C}$

Now this reduces to :-

$$A.\overline{B}(C + \overline{C}) = A.\overline{B}.1 = A.\overline{B}$$

and this looks like the system shown in the lower part of the diagram. The reason for the simplification is that C and $\overline{C}$ occur in the same output and cancel out.

Thus $C + \overline{C} = 1$ means that there will be an output irrespective of the state of C. The switching is thus minimised to $A.\overline{B}$ as these two terms are common to both parts of the expression. This may be obvious here but in a large system may easily be overlooked.

Other Boolean functions can be seen to be true in

terms of switches. For example, $A.\overline{A} = 0$ - there is never any output.

Logic Polarity

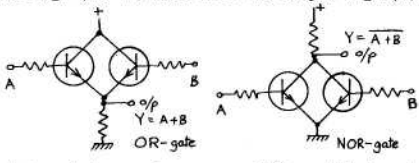
Switching logic is one way to make AND and OR type systems but another is to use Digital Integrated Circuits. These are specially designed for the job and carry the appropriate names like AND, NAND, NOR, etc.

Before describing IC gates, as they are called, the actual logic system has to be clarified.

Since digital logic is concerned with two states it follows that there are two ways of defining the 0 and 1 conditions. In electronics voltage is usual and 1 means some voltage and 0 means no voltage, but this can be confusing when positive and negative voltages are used. To overcome the problem Positive Logic is defined as being in the 1 state when the voltage is more positive than than the other state which is then called 0. Negative logic is defined as being 1 when the voltage is more negative. So negative logic is the inverse of positive logic i.e. the 1s and 0s interchange. Positive logic is the usual convention.

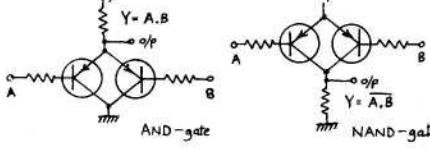
Gates

A gate is said to be a system which performs an AND or OR type of function. A simple positive-logic gate is shown. It is an OR-gate because either A OR B taken high (to +) will make the output high (1).



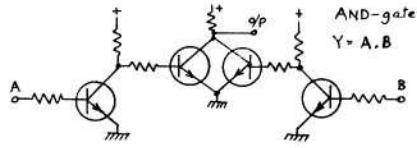
A transistor used as an amplifier will invert and provide the NOT function. So two paralleled amplifiers will make a NOT-OR gate, or NOR-gate. $Y = \overline{A + B}$

The next diagram shows a way to make an AND-gate. Both transistors must be OFF for the output to be high. If amplifiers are used we get a NAND-gate as expected.



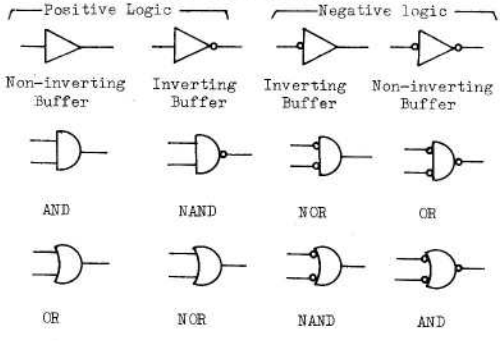
If the transistors are restricted to all npn types (as in a TTL IC) then the AND and NAND must be obtained in a different manner. If the inputs are inverted to a NOR-gate the result is seen to be the same as if an AND-gate had been used because:-

$\overline{\overline{A} + \overline{B}} = A.B$ by using Boolean Algebra (De Morgans theorem)



A NAND-gate can be made in a similar fashion.

Now all this circuitry is tedious and unnecessary so it is simplified to symbols as shown below. Note, there are several conventions for doing this simple little task and only one is shown. It is more or less the same as the manufacturer's convention and is used throughout this series of articles.



The small circles denote inversion. If they appear at the inputs to a device it signifies that the device is handling negative logic although it is a positive logic device. Each of the functions shown above appears twice. This is because of the two logic conventions - the AND-gate can be made either from a positive-logic AND-gate or a negative-logic OR-gate (with inversions before and after). This follows from De Morgan's theorem where $\overline{A.B} = \overline{A} + \overline{B}$, and similarly for the other functions.

A close examination of manufacturers' data for TTL ICs will reveal all the above functions.

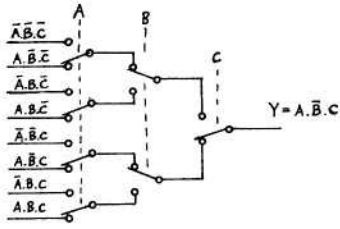
Of course more than two inputs can be used - up to eight (or more with wired-OR). It is not necessary to know what is inside the gates as a digital circuit can be drawn entirely with these symbols. The logic thus applies whatever the type of gate; whether it be RTL, DTL, TTL, ECL or CMOS, etc.

When several inputs are used it is often difficult to visualise what the output is going to do for the input combinations. This can be made clear if a truth table is set out.

Truth Tables

A switching tree can be arranged to provide all the possible combinations of n variables (three in the diagram).

This is rather cumbersome to draw and can be equally well represented by a table. The one shown indicates that there is an output only if the switches are in the positions A.$\overline{B}$.C.



C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Such a table is called a truth table and is normally arranged in binary sequence with the most significant bit at the left. There are eight combinations of three variables, all of which appear in the table. The output Y is a 1 only when the logic agrees with the Boolean function A.B.C.

Having got the various inputs into a table we can now see what some of the basic functions look like.

AND

A	B	Y
0	0	0.0=0
0	1	0.1=0
1	0	1.0=0
1	1	1.1=1

A.B

OR

A	B	Y
0	0	0+0=0
0	1	0+1=1
1	0	1+0=1
1	1	1+1=1

A+B

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$\overline{A.B}$

These show quite clearly how Boolean Algebra can describe a function.

So now not only can we write down logic in Boolean form but we can also tabulate existing logic and work out the appropriate Boolean expression straight from a truth table.

The next truth table shows what a particular circuit is doing. What is the Boolean expression?

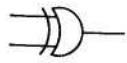
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Well the Y column gives two 1s which means that there are two cases where the inputs provide an output. These are for $\overline{A}$.B and A.$\overline{B}$. Since there are two we can say there is an output if $\overline{A}$.B OR A.$\overline{B}$ is present. The expression is :-

$Y = \overline{A}.B + A.\overline{B}$

As it happens this particular function has a special name - Exclusive-OR. This is because it is the OR function with the AND function removed (AND has the 1.1 condition as 1 - see above). The OR function should really be called the Inclusive-OR function because it includes AND but it almost never is.

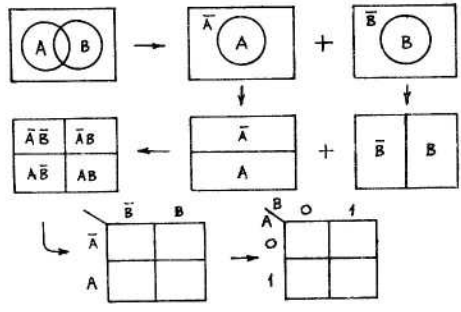
The Exclusive-OR function is found as a special device in TTL and also has a special symbol and a special sign in Boolean form. Thus $\overline{A}.B + A.\overline{B} = A \oplus B$



The Exclusive-OR gate is a very useful piece of logic as it forms part of a Binary Adder and it turns up all over the place in logic systems.

Karnaugh Maps

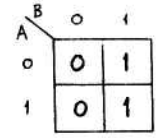
If a Venn diagram is altered into a rectangular shape it can be made much more useful. This is shown below for a two-variable diagram.



Any function with two variables can now be plotted on this diagram, or, map as it is called after M. Karnaugh who invented the arrangement. This map shows all the locations of the Y outputs for an expression and a 1 identifies a particular subset. Not only can any Boolean function be plotted but any truth table can be transferred to it also.

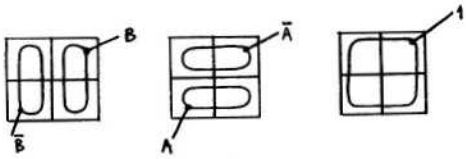
This map now has two advantages over a Venn diagram; it can handle more than three variables (as will be seen shortly) and it is arranged so that minimisation of the appropriate Boolean expression is easily achieved without any calculations.

For instance, if the expression A.B + $\overline{A}$.B is plotted we get:-



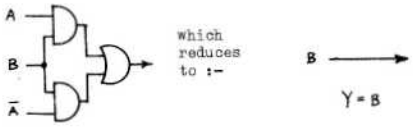
Now, from Boolean Algebra we know that A.B + $\overline{A}$.B = (A + $\overline{A}$)B and since A + $\overline{A}$ = 1 this reduces to B. If we look at the map, the two 1s are seen to be vertically adjacent. They therefore cover both states of A and we can get the answer of B by knowing this fact.

Taken another way, the map is known to have areas which correspond to basic expressions and so if the 1s fit such an area exactly then the total expression can be said to be equivalent to the basic expression. The basic areas for a two-variable map are now shown. Note that they correspond to the coding along the edges of the map



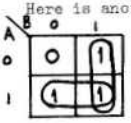
The basic areas are ringed around with loops and the rules for making these loops are seen to be simple - they must be rectangular or square with a binary number of squares along each side.(1,2,4,8 etc.)

If we now again look at the map of $A.B + A.\bar{B}$ it can be seen immediately that the loop around the two 1s is equivalent to B, and this can straightaway be written down. In a practical form this is :-



This is a considerable reduction of logic which may not have been obvious at first sight.

Here is another example; this time for an OR function.



The expression is A + B because there are two loops, each of which represents a basic expression.

It is not essential to use the 1s, we could use the 0s in which case the answer would be negative. For the same example 0 represents the expression :-

$\bar{Y} = \bar{A}.\bar{B}$ or $Y = \overline{\bar{A}.\bar{B}}$

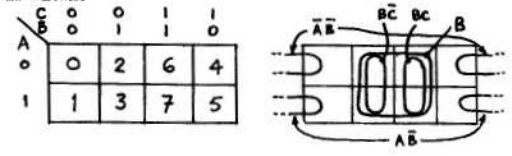
From De Morgan's theorem $\overline{A.B} = \bar{A} + \bar{B}$

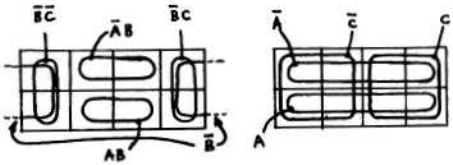
so $\overline{\bar{A}.\bar{B}} = A + B$

WHICH IS EXACTLY THE SAME as before (and incidentally a proof of De Morgan's theorem).

This equality thus states that a negative logic NAND is the same as a Positive logic OR.

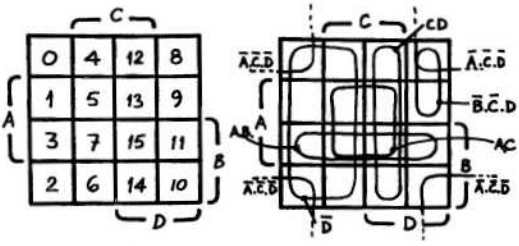
So far the Karnaugh map is not a lot of use but as the number of variables is increased it does become of use. A three-variable map is now shown. It need not be a horizontal rectangle; it could be vertical or even a strip of eight squares, but it is easier to deal with as shown.





The numbers in the squares show the order in which they are filled-in from a binary sequence - as in a truth table. This is shown by the coding at the sides. Incidentally, it is not important which variable goes where, only the order in which the combinations are put down matters. That is, the sequence along the sides MUST be such that from one square to the next there is a difference of only one bit. In other words a Gray code. The map can be considered to be rolled into a cylinder so that the first and last combinations are together - and still only differ by a single bit. The RHS of the map is now seen to be a mirror-image of the LHS. Each adjacent square thus differs by the negation of a single bit. For example, from $A.B.\bar{C}$ to $A.B.C$ (squares 3 to 7) the only difference is the negation of C. If a loop were drawn around these two terms only the resulting expression would thus be A.B

A four-variable map is now shown together with some loops - the rest being omitted for clarity. The edge coding is also shown in a simpler manner. This map is twice the size of a three-variable map and the RHS is again a mirror-image of the LHS. Also the top is a mirror-image of the bottom. Larger maps for more variables can be constructed along these lines - doubling for each additional variable.



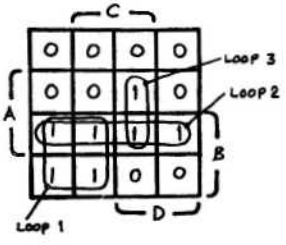
An example of the use of such a map in reducing the complexity of logic is now given. Supposing we have a requirement that an output is required from various systems such that the following equation is satisfied:-

$$Y = \bar{A}.B.\bar{C}.\bar{D} + A.B.\bar{C}.D + \bar{A}.B.C.\bar{D}. + A.B.C.\bar{D} + A.B.\bar{C}.D + A.\bar{B}.C.D + A.B.C.D$$

This is quite a formidable task to achieve by Boolean Algebra but by the use of a map can be done in a few moments.

There are only four variables so the map has sixteen squares. The seven groups correspond to seven of these squares and these must have a 1 put in them. Since no

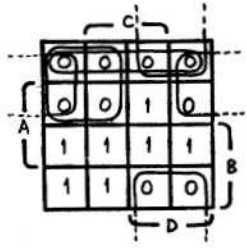
other output must result from any other combination of the four variables, all the other squares must contain Os. Now we draw in loops so as to ring the 1s. Each loop must be as large as possible and several loops may ring a particular 1 if need be; bearing in mind the sizes and shapes previously mentioned for the loops.



Three loops can be drawn. Loop 1 is equivalent to $B.\overline{D}$, loop 2 to A.B and loop 3 to A.C.D. No other 1s are left and no other loops can be drawn so the resulting expression has three parts :-

$$Y = B.\overline{D} + A.B + A.C.D$$

Simple isn't it? The same expression could have been reached by using only the Os and then using De Morgan's theorem to convert it:-



Surprisingly there are only four loops giving :-

$$Y = \overline{\overline{B.\overline{D}} + \overline{A.\overline{B}} + \overline{B.\overline{C}} + \overline{A.D}}$$

This might be easier to implement in the form of logic gates but is the same the previous expression.

Proof by Boolean Algebra :-

$$\overline{\overline{B.\overline{D}} + \overline{A.\overline{B}} + \overline{B.\overline{C}} + \overline{A.D}} = (\overline{B.\overline{D}})(\overline{A.\overline{B}})(\overline{B.\overline{C}})(\overline{A.D}) \quad \text{By De Morgan}$$

$$= (B + D)(A + B)(B + C)(A + \overline{D})$$

Multiplying out $= (A.B + A.D + B + B.D)(A.B + A.C + B.\overline{D} + C.\overline{D})$

This is $= A.B + A.B.C + A.B.\overline{D} + A.B.C.\overline{D} + A.B.D + A.C.D + A.B.D.\overline{D} + A.C.D.\overline{D}. + A.B. + A.B.C + B.\overline{D} + B.C.\overline{D} + A.B.D + A.B.C.D + B.D.\overline{D} + B.C.D.\overline{D}$

By eliminating zero terms this becomes ;

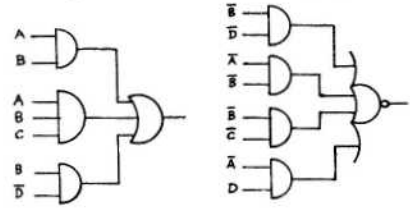
$$A.B + A.B.C + A.B.\overline{D} + A.B.C.\overline{D} + A.B.D + A.C.D + B.\overline{D}. + B.C.\overline{D} + A.B.C.D$$

This reduces to $A.B + A.B.C. + A.C.D + B.\overline{D} + B.C.\overline{D}$

and again to $A.B + A.C.D + B.\overline{D}$

So the two methods do give the same answer. This is very much easier than manipulating all those Boolean expressions as just shown. It is all too easy to miss a bar and end up with a frightful result.

The two methods of solving the problem can be realised in practical form as shown below.



The O-case is not simpler in this instance but it may well have been - particularly if there had been less Os than 1s. It all depends on how the loops can be formed.

Checking Minimisation

Although Karnaugh Maps can be used to minimise logic with ease, it is still possible to make mistakes. A method of checking is required and this takes the form of a truth table in which the various expressions are set out. They can then be checked before and after minimisation. For example :-

$$\overline{A}.B.\overline{C}.\overline{D} + A.B.\overline{C}.\overline{D} + \overline{A}.B.C.\overline{D} + A.B.C.\overline{D} + A.B.\overline{C}.D + A.\overline{B}.C.D + A.B.C.D = B.\overline{D} + A.B + A.C.D \quad \text{or} \quad \overline{\overline{B.\overline{D}} + \overline{A.\overline{B}} + \overline{B.\overline{C}} + \overline{A.D}}$$

D	C	B	A	B.D	A.B	A.C.D	sum	B.D	A.B	B.C	A.D	sum	$\overline{\text{sum}}$
0	0	0	0	0	0	0	0	1	1	1	0	1	0
0	0	0	1	0	0	0	0	1	0	1	0	1	0
*0	0	1	0	1	0	0	1	0	0	0	0	0	1
*0	0	1	1	1	1	0	1	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1	0	0	1	0
0	1	0	1	0	0	0	0	1	0	0	0	1	0
*0	1	1	0	1	0	0	1	0	0	0	0	0	1
*0	1	1	1	1	1	0	1	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	1	1	1	1	0
1	0	0	1	0	0	0	0	0	0	1	0	1	0
1	0	1	0	0	0	0	0	0	0	0	1	1	0
*1	0	1	1	0	1	0	1	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	1	0	1	1	0
*1	1	0	1	0	0	1	1	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	0	1	1	0
*1	1	1	1	0	1	1	1	0	0	0	0	0	1

* The seven LHS terms are indicated by stars.

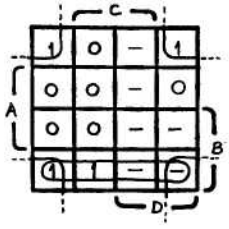
The two 'sum' columns have 1s which match the starred terms so the equations balance and the expressions are equivalent.

Examples of Karnaugh Map Minimisation

Now for an example that also incorporates 'don't care' conditions. These occur when the required combinations will never be encountered and this fact can be put to use to simplify the logic.

The 7448 7-segment decoder has a mass of logic inside it. We are going to examine the logic required to operate the 'e' segment. The truth table shows the segment to be illuminated when a 1 is present in the RH column. There are six 'don't care conditions in which the indicator is not required to show a number (it does in fact show a shape). This does not matter as these six numbers will not normally occur.

Dec.	Bin D	C	B	A	'e'
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	-
11	1	0	1	1	-
12	1	1	0	0	-
13	1	1	0	1	-
14	1	1	1	0	-
15	1	1	1	1	-



The six 'don't cares' and the 1s and 0s are all plotted on a four-variable Karnaugh map and loops drawn around the 1s as before; but this time the 'don't cares' are treated as though they were 1s and included in the loops.

The expression for this map can now be written down from the two loops :-

$$Y = \overline{A}.B + \overline{A}.\overline{C}$$

Looping the 0s gives $Y = \overline{A + \overline{B}.C}$ which is the same:

$\overline{A}.B + \overline{A}.\overline{C} = \overline{A}(B + \overline{C}) = \overline{A + (\overline{B + C})} = \overline{A + \overline{B}.C}$

A look at the manufacturer's data will show the logic. CQ-TV 82, page 22 and 23 also show the logic - but note that the 7446 has opposite polarity outputs from the 7448 so that one inversion is missing from the diagram on page 22.

The next example shows how to design a Synchronous Counter to generate a 4-bit Gray code of 10 states (where only one bit changes at a time). The required sequence is given in a truth table. Note that it is not in a binary sequence and the count numbers are not binary equivalents.

Examination of the table shows that D changes from 0 to 1 after the first clock pulse. This can be achieved in a JK bistable by providing the J-input at the time of the 0000 with a 1. The first pulse then makes D_Q a 1. (The operation of a J-K bistable is described in CQ-TV 83.)

The next pulse must not change D so the K-input must be 0 during the 1000 state. After the third pulse the D-output returns to 0 so that the K-input must have been a 1 during the 1100 state. The D-output then stays at 0 for three more states so that the J-input must be at 0 for three states, and so on. The J and K input requirements are shown in the eight columns alongside the input codes in the truth table.

Count	D	C	B	A	D_J	D_K	C_J	C_K	B_J	B_K	A_J	A_K
0	0	0	0	0	1	-	0	-	0	-	0	-
1	1	0	0	0	-	0	1	-	0	-	0	-
2	1	1	0	0	-	1	-	0	0	-	0	-
3	0	1	0	0	0	-	-	0	1	-	0	-
4	0	1	1	0	0	-	-	0	-	0	1	-
5	0	1	1	1	0	-	-	0	-	1	-	0
6	0	1	0	1	1	-	-	0	0	-	-	0
7	1	1	0	1	-	0	-	1	0	-	-	0
8	1	0	0	1	-	1	0	-	0	-	-	0
9	0	0	0	1	0	-	0	-	0	-	-	1

It will be seen that there are a lot of 'don't care' states in the J and K requirements and these can be used to advantage in the Karnaugh maps. Generally, the J and K columns alternate such that the J matches the 0s in the state columns whilst the K matches the 1s. Any change is shown by the 0 to 1 change in the J and K columns.

Eight maps are required as there are four J and four K inputs - there are four bistables because there are four variables.

To ease matters a single map is drawn first to show where the states fit in the order of the count. The eight maps are now easy to compile from the truth table. They are :-

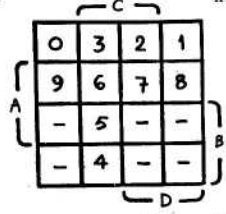
The resulting expressions are :-

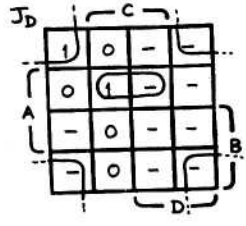
$$J_D = \overline{A}.\overline{C} + A.\overline{B}.C \qquad K_D = A.\overline{C} + \overline{A}.C$$

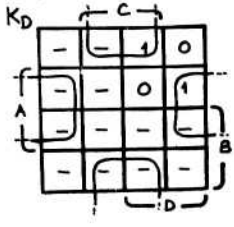
$$J_C = \overline{A}.D \qquad K_C = A.D$$

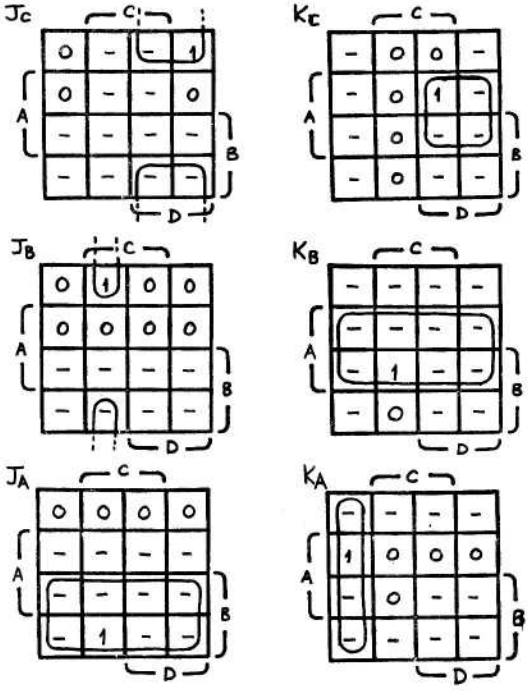
$$J_B = \overline{A}.C.\overline{D} \qquad K_B = A$$

$$J_A = B \qquad K_A = \overline{C}.\overline{D}$$

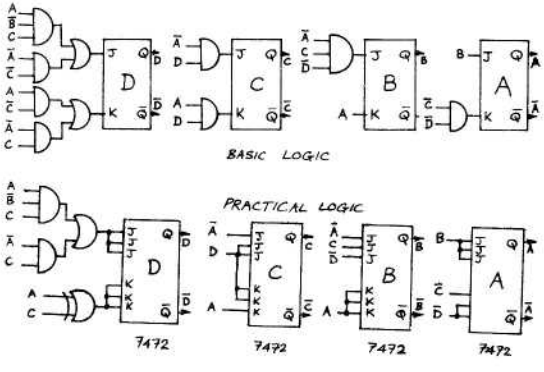






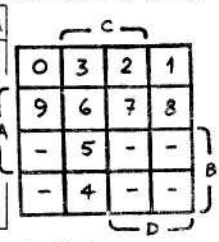


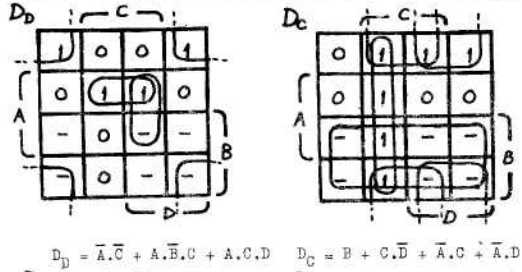
The resulting expressions can be assembled in logic form and then again in more practical form as shown below. Only the 1s were looped in this example as there are fewer 1s than 0s which results in simpler logic.



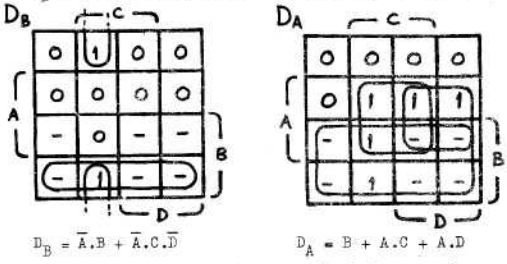
If we do the same with D-bistables can we expect the logic to be simpler? At first sight it ought to be since there are only four data inputs to the bistables instead of eight, but the truth table reveals that there are no don't care states and the logic is going to be more complex as a result since the expressions will not reduce so easily.

Count	D C B A	D_D	D_C	D_B	D_A
0	0 0 0 0	1	0	0	0
1	1 0 0 0	1	1	0	0
2	1 1 0 0	0	1	0	0
3	0 1 0 0	0	1	1	0
4	0 1 1 0	0	1	1	1
5	0 1 1 1	0	1	0	1
6	0 1 0 1	1	1	0	1
7	1 1 0 1	1	0	0	1
8	1 0 0 1	0	0	0	1
9	0 0 0 1	0	0	0	0



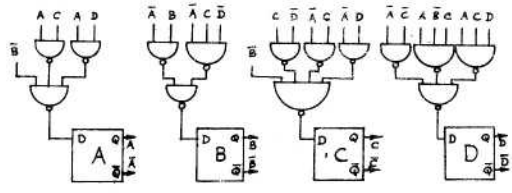


$D_D = \bar{A}.\bar{C} + A.\bar{B}.C + A.C.D$ $D_C = B + C.\bar{D} + \bar{A}.C + \bar{A}.D$



$D_B = \bar{A}.B + \bar{A}.C.\bar{D}$ $D_A = B + A.C + A.D$

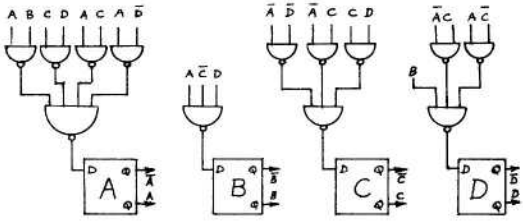
The logic is implemented in practical form as shown:-



Note, the 7474's require invertors according to the expressions so to save these the Q and $\bar{Q}$ outputs were swopped over instead - and hence ALL the logic polarities.

This shows that the D-bistable version, whilst easier to work out, is actually more difficult to realise in practical terms. This is often the case and JK bistables usually give a simpler system because triple inputs are available for J and K. Also the 'don't care' states help the reduction considerably.

If Os are looped it works out to this:-

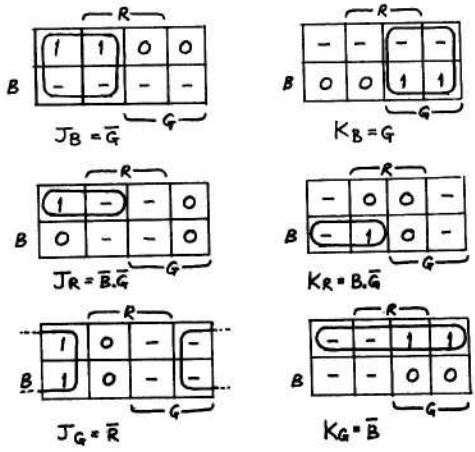


The final example is the logic required to generate Colour Bars in Phase sequence - see CQ-TV 75 page 23. This is basically an eight-step counter and the truth table is :-

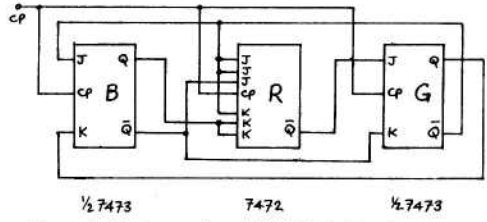
Colour	Sequence	Blue	Red	Green	J_B K_B	J_R K_R	J_G K_G
White	0	1	1	1	- 1	- 0	— 0
Yellow	1	0	1	1	0 -	- 0	- 1
Red	2	0	1	0	1 -	- 0	0 -
Magenta	3	1	1	0	- 0	- 1	0 -
Blue	4	1	0	0	- 0	0 -	1 -
Cyan	5	1	0	1	- 1	0 -	- 0
Green	6	0	0	1	0 -	0 -	- 1
Black	7	0	0	0	1 -	1 -	1 -

The sequence map and the six Karnaugh maps are:-

7	2	1	6
4	3	0	5



The resulting logic is implemented as follows :-



The eqivalent version with D-bistables is more complex and so will not be shown here.

These various examples have demonstrated that Karnaugh map reductions form a powerful tool when designing logic circuits. Logic, Binary codes, gates, maps, etc., can all be used to advantage in digital circuitry to simplify design procedures which would otherwise take hours to do.

This article completes the series as far as TTL ICs are concerned although the content of the article applies to all kinds of logic systems. Future parts in the series will cover CMOS, Linear ICs and more Operational Amplifier applications as well as possibly mentioning certain more specialised ICs such as memories and Consumer ICs.

The content of the TTL articles will shortly be turned into a booklet - when I can find the time.

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